Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **Vcc**

**71**

**32**

**5 4 3 2**

**9 10 11 12**

**1**

**14**

**13**

**6**

**7**

**8**

**MASK**

**REF**

**.049”**

**.017”**

**A**

**B**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 7132**

**APPROVED BY: DK DIE SIZE .047” X .049” DATE: 12/17/18**

**MFG: T.I. /NATIONAL SEMI THICKNESS .015” P/N: SN74132**

**DG 10.1.2**

#### Rev B, 7/19/02